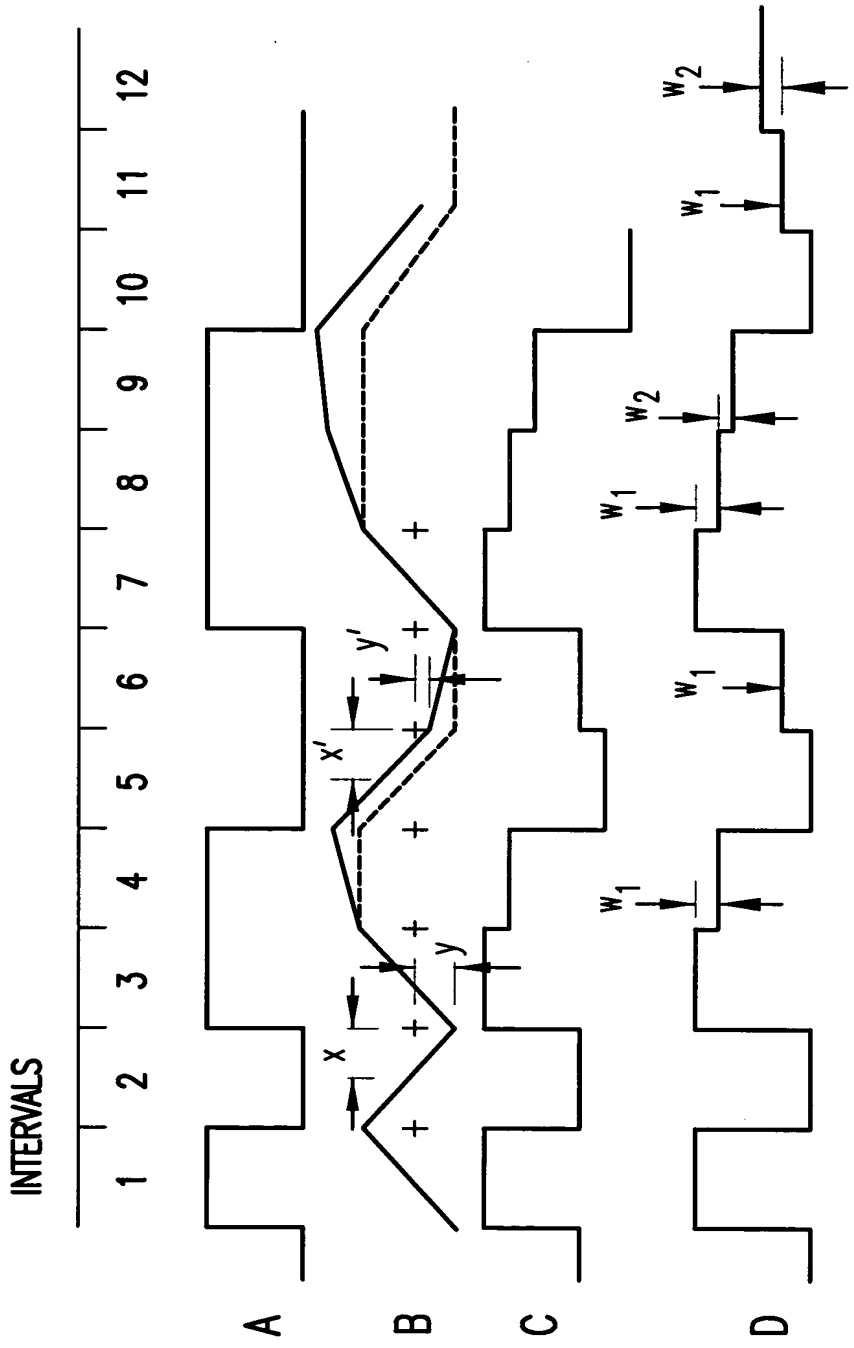

FIG.1

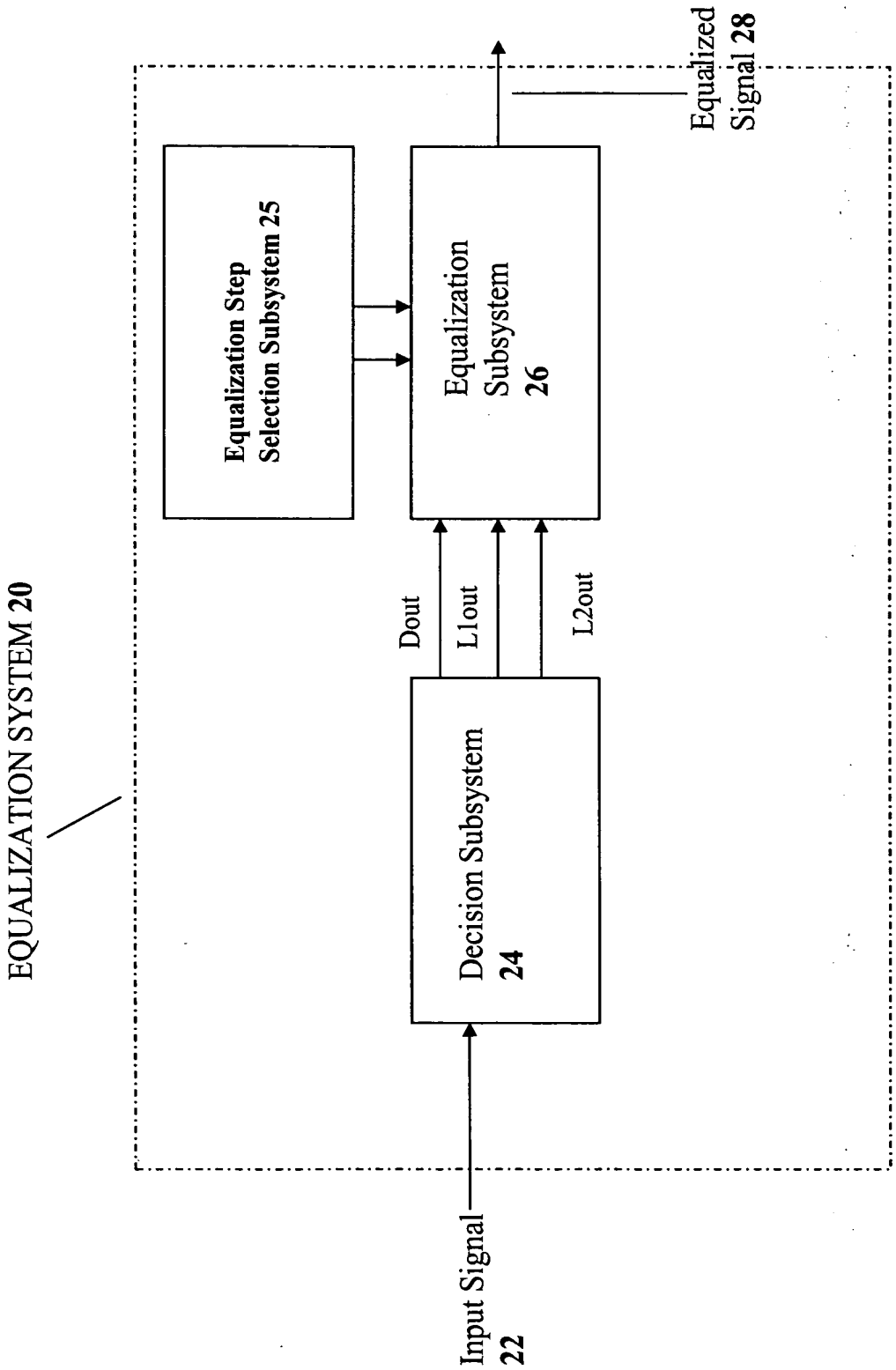
EQUALIZATION SYSTEM 20
Equalization Step Selection Subsystem 25
Equalization Subsystem 26
Equalized Signal 28
Decision Subsystem 24
Dout
L1out
L2out
Input Signal 22

Fig. 2

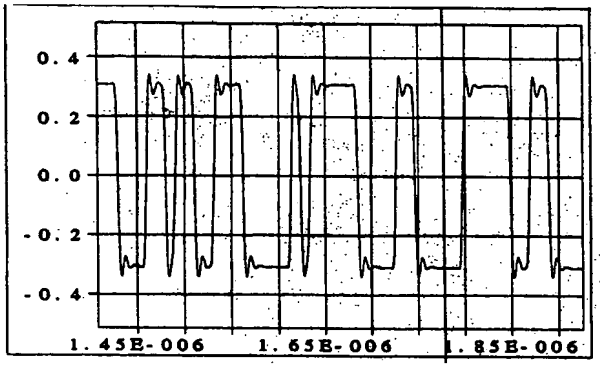

Fig. 3(a)

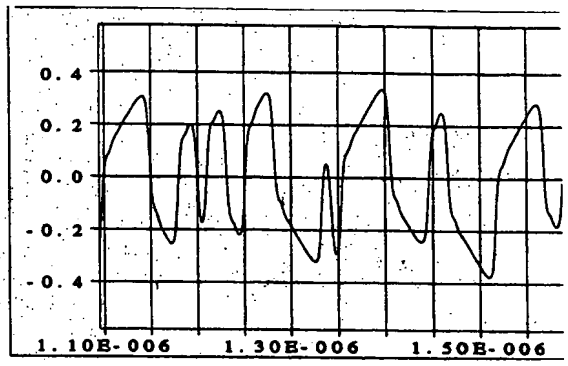

Fig. 3(b)

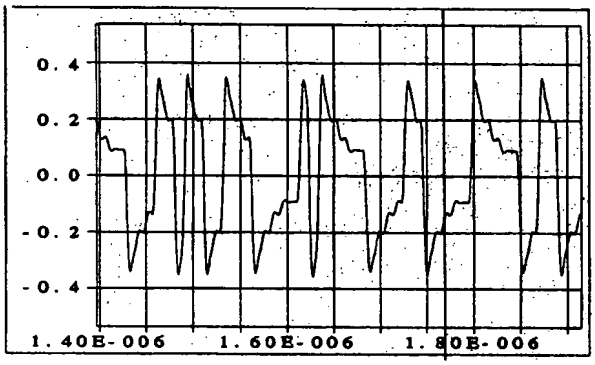

Fig. 4(a)

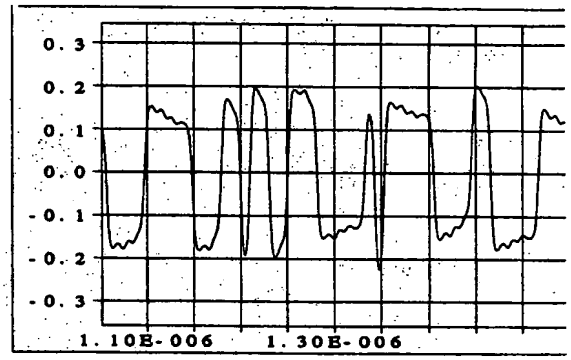

Fig. 4(b)

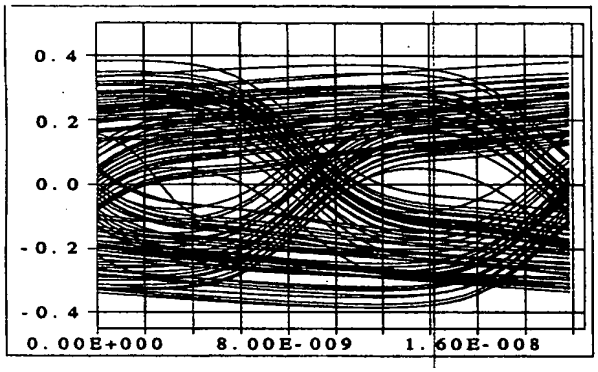
0.4
0.2
0.0
-0.2
-0.4
0.00E+000
8.00E-009
1.60E-008

Fig. 5(a)

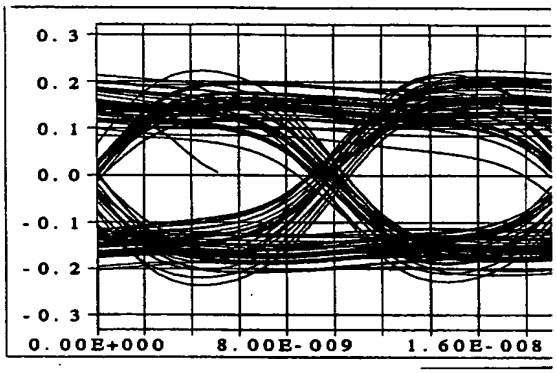
0.3
0.2
0.1
0.0
-0.1
-0.2
-0.3
0.00E+000
8.00E-009
1.60E-008

Fig. 5(b)

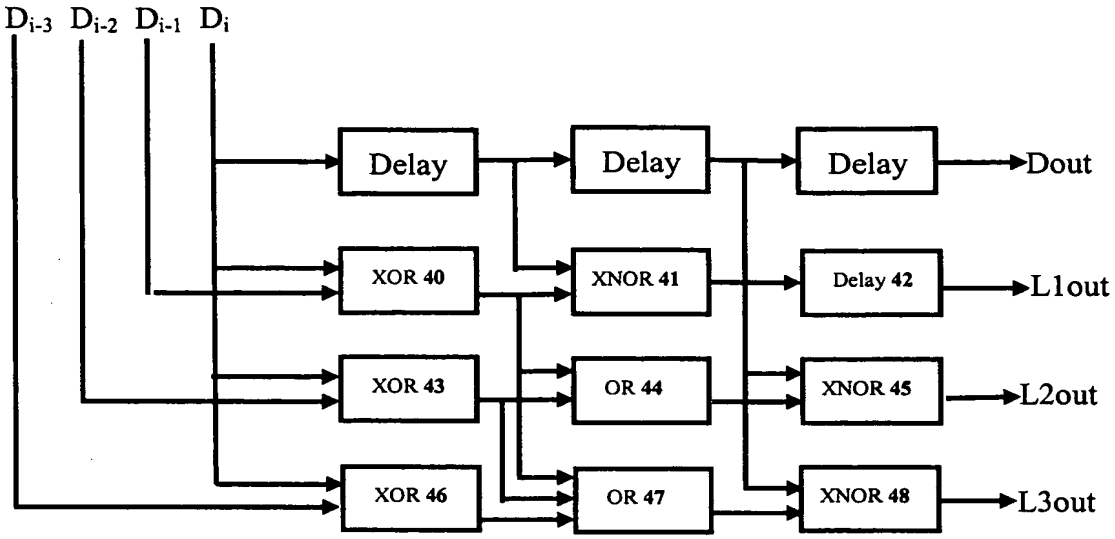

Fig. 6 A block diagram for the equalization logic that generates the three signals levels

Sample Input Stream = 01000111100 (a = MSB; b = first to right of MSB; k = LSB)
a = 0; b = 1; c = 0; d = 0; e = 0; f = 1; g = 1; h = 1; I = 1; j = 0; k = 0

Bit Identity	Dout	L1out	L2out	L3out
a	0	--------	----------	----------
b	1	1	1	1
c	0	0	0	0
d	0	1	0	0
e	0	1	1	0
f	1	1	1	1
g	1	0	1	1
h	1	0	0	1
I	1	0	0	0
j	0	0	0	0
k	0	1	0	0

Fig. 7

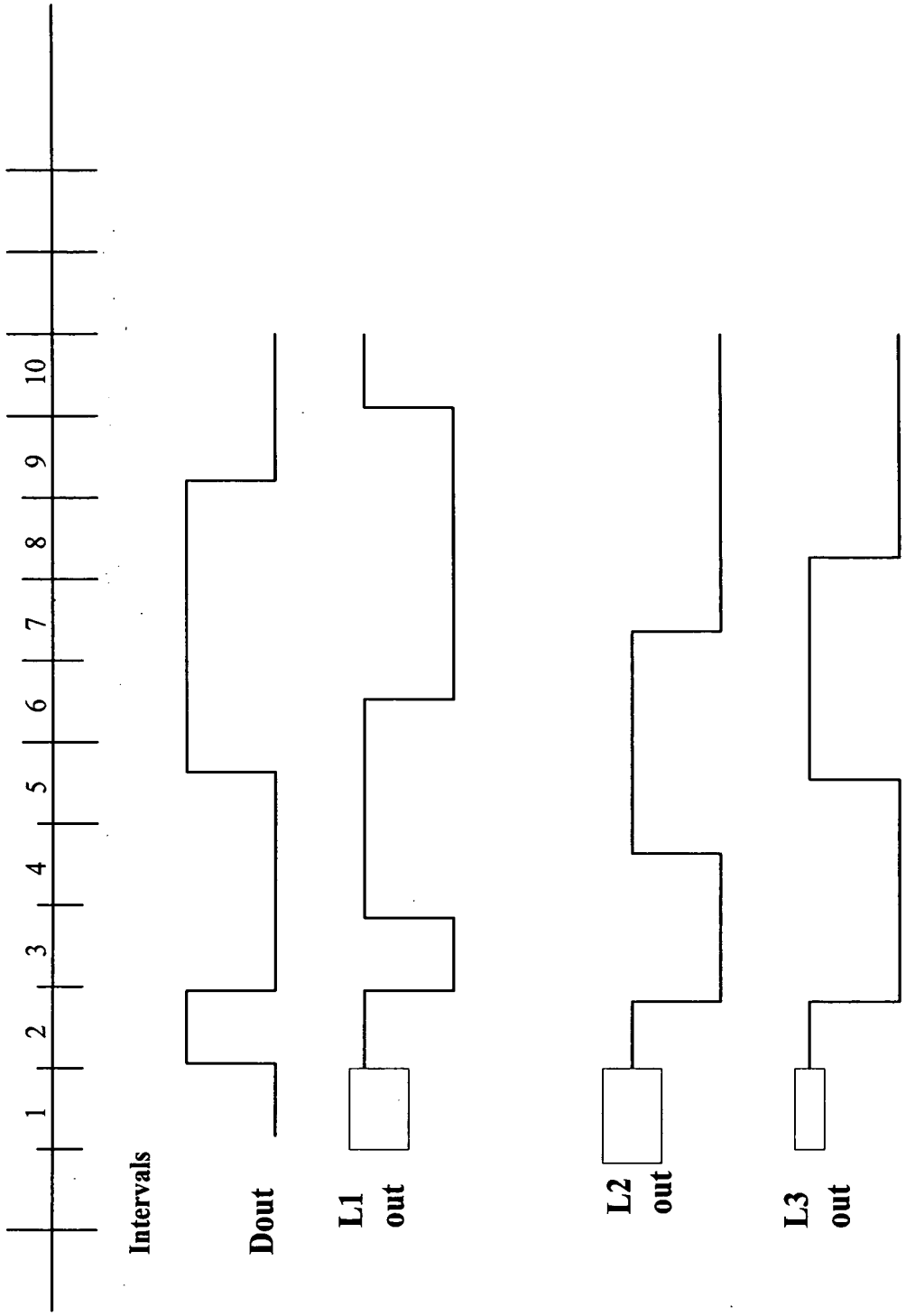

Fig. 8

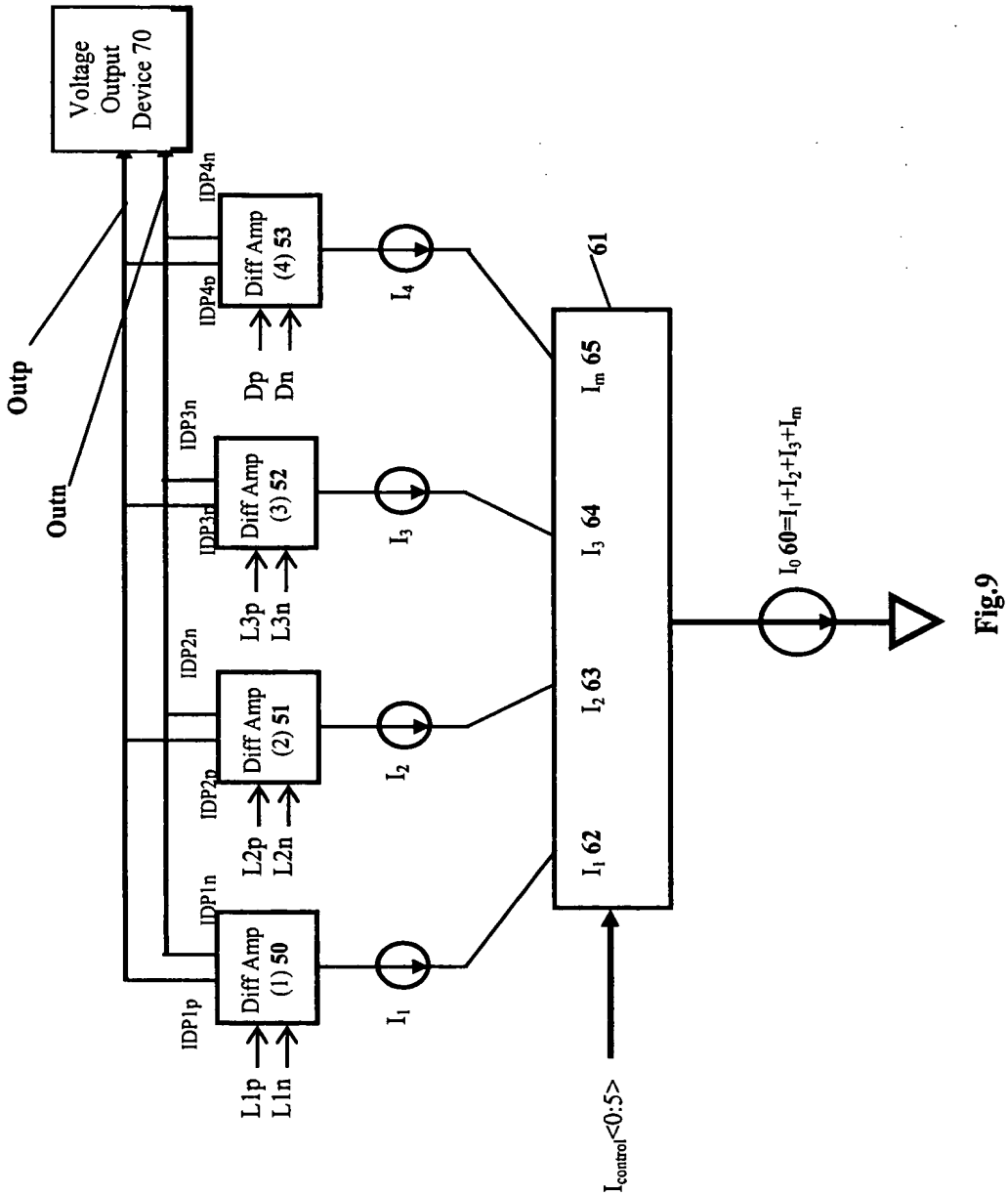
Voltage Output Device 70
Outp
Outn
Diff Amp (1) 50
Diff Amp (2) 51
Diff Amp (3) 52
Diff Amp (4) 53
IDP1p
IDP1n
IDP2p
IDP2n
IDP3p
IDP3n
IDP4p
IDP4n
L1p
L1n
L2p
L2n
L3p
L3n
Dp
Dn
I1
I2
I3
I4
61
I1 62
I2 63
I3 64
Im 65
I0 60=I1+I2+I3+Im
Icontrol<0:5>

Fig.9

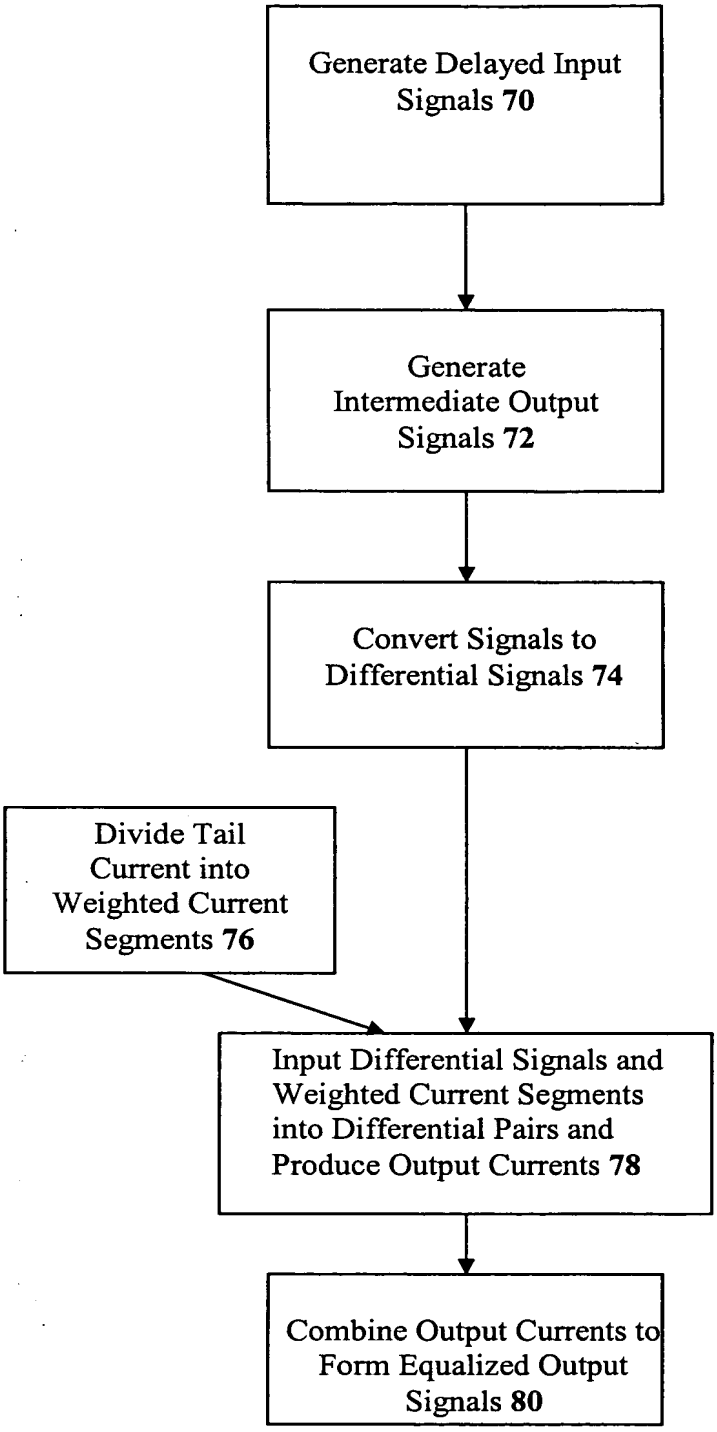
Generate Delayed Input Signals 70
Generate Intermediate Output Signals 72
Convert Signals to Differential Signals 74
Divide Tail Current into Weighted Current Segments 76
Input Differential Signals and Weighted Current Segments into Differential Pairs and Produce Output Currents 78
Combine Output Currents to Form Equalized Output Signals 80

Fig. 10